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Reduced Comparator Flash ADC for ECG Applications

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Abstract **- A CMOS based low power 4-bit Flash Analog to Digital Converter (ADC) design with reduced number of comparators than the conventional Flash Analog to Digital Converter and multiplexer based architecture is proposed. For improving the conversion rate, both the analog and digital parts of the ADC are fully modified and the architecture uses only 4 comparators instead of 15 as used in conventional flash ADC, thus saving considerable amount of power. The proposed 4-bit ADC is designed and simulated in TANNER tools with 1.2 V supply voltage using TSpice simulation. The proposed design consumes low power of 2.15mW and operates at a faster rate hence it is suitable for ECG applications.**

Keywords **– Flash ADC, Comparators, CMOS, TANNER.**

I. INTRODUCTION

The performance of biomedical data acquisition systems such as ECG is generally limited by precision of the digital input data, which is achieved at the interface between analog and digital signals. ECG is a common bio-potential signal with low amplitudes of 1000-10000μV and low frequency of 0.5-100Hz [1]. In ECG applications the design with minimum power dissipation is always the key while fabricating the integrated circuit for such an ADC. The most prominent drawback of flash ADC is the fact that the number of comparators grows exponentially with the number of bits [2]. Increasing the quantity of the comparators also increases the area of the circuit, as well as the power consumption.

Successive approximation architectures which have a logarithmic dependence on resolution are alternative approaches to reduce the complexity and the power consumption of flash ADC. On the other hand, it's not desirable to use those kinds of ADCs in high-speed applications since they consume multiple clock cycles to implement the conversion algorithm, which needs more time interleaving to increase the conversion speed[2].

The main concern of this paper is to reduce the power consumption for flash ADC to be suitable for usage in low voltage applications. Flash ADCs are still the architecture of choice, where maximum sample rate and low to moderate resolution is required [3].

Speed, resolution and power dissipation are the three main parameters for ADC [4] and they can't be changed once an ADC is designed. This paper presents a CMOS based 4-bit ADC that uses only 4comparatorsinstead of 15 comparators so it dissipates minimum power and can operate at higher speed at low resolution. This paper is organized into 5 sections.

The conventional flash ADC is reviewed in Section II. The proposed flash ADC is presented in Section III. Simulation results are demonstrated in Section IV. Conclusions are drawn in Section V.

II. CONVENTIONAL FLASH ADC

A block diagram of a conventional N-bit flash ADC is shown in Fig.1.For an N bit Flash Analog to Digital converter the circuit employs 2^N-1 comparators. A resistive divider with 2^Nresistors provides the reference voltage. These voltages are compared with the analog input signal in just one clock cycle. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Each comparator produces a "1" when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator output is "0".These voltages are compared with the analog input signal in just one clock cycle.

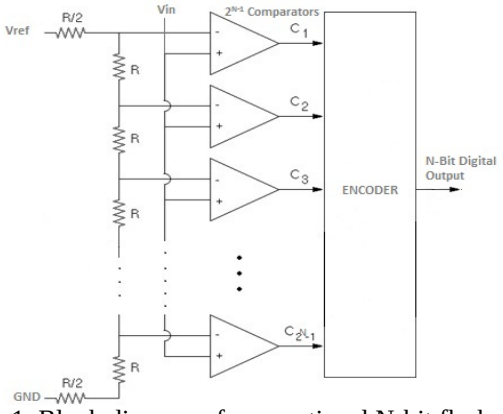

Fig.1. Block diagram of conventional N-bit flash ADC

Some of the problems of the conventional comparator structures used in ADC designs are [5]:

1. Large transistor area for higher accuracy
2. DC bias requirement
3. Charge injection errors
4. Metastability errors
5. High power consumption
6. Resistor or capacitor array requirement.

The encoder is used to convert the thermometer code, generated by the comparators into a binary code that approximates the input signal. The cyclic encoder detects the pair of 1-0 and 0-1 location and converts it to binary.

III. PROPOSED FLASH ADC

The block diagram of proposed 4-bit flash ADC is shown in Fig.2. It uses multiplexer and reduced number of comparator for ADC operation. The multiplexer is used for generation of reference voltages while the comparators are used for comparing different reference voltages.

In comparison to the conventional flash ADC which uses 2^N-1 comparators for N- bit ADC, the proposed one uses only N comparators and N-1 multiplexers to generate the required binary code resulting in saving of power and area.

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The principle behind this proposed work is to use analog multiplexer to change the reference voltage in accordance to the previous significant bit and to exploit the properties of comparators. As comparators are the fast element and consume most of the power hence to reduce the power, the reduction of comparators is the only alternative and the proposed design follows the same path.

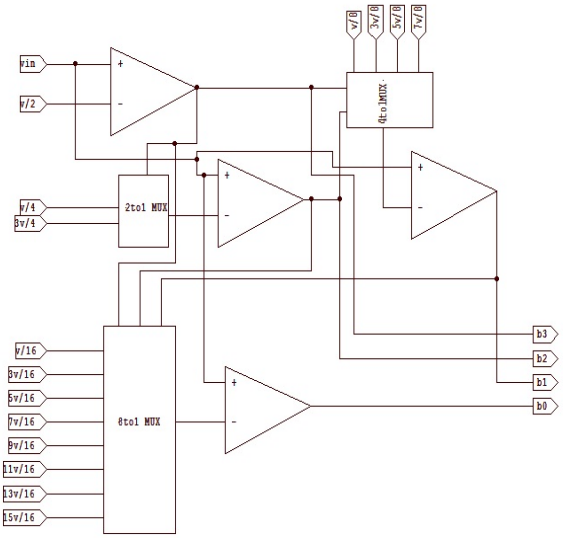

Fig.2. Block diagram of 4-bit flash ADC

The most significant part of ADC architecture is comparator. Comparator is a circuit that compares two analog input signals and decodes the signal into single digital output signal. Flash type ADC usually referred as direct conversion ADC has a bank of comparators sampling the input signal in parallel, each firing for their decoded voltage range. Direct conversion is very fast, capable of gigahertz sampling rate. The schematic design of comparator is shown in Fig.3.The input voltage is compared with the reference voltage and the output is 1 when input voltage is greater than the reference voltage. Output is 0 when input voltage is lesser than the reference voltage.

In comparator there are two stages, first stage is composite cascode differential amplifier N channel input devices in series with combination of cascode active PMOS based current mirror load that compares the two input but provide smaller gain while the second stage is common source provide larger swing and greater gain similar to op-amp based conventional two stage open loop comparator and one NMOS is provided below which act as current sink for stabilization. Amplifiers are usually employed to achieve linear operation in closed loop configuration which requires careful compensation to avoid unstable operation [6]. On the contrary the comparator does not require stability criteria as in two stage amplifier so it eliminated need for compensation capacitor.For providing different reference voltages to the comparator, CMOS based transmission gate is used as analog multiplexer. Multiplexers are key components in CMOS memory elements and data manipulation structures. A multiplexer chooses the output from among several inputs based on a select signal. The conventional multiplexer has at least two inputs, at least one output and at least one control select line terminal. Each of the inputs is associated with a separate and distinct path through the multiplexer. One source terminal of the multiplexer circuit is connected to high voltage source V_{dd}. Another source terminal is connected to ground or V_{ss}. The conventional multiplexer are mostly built in complementary metal-oxide-semiconductor technology to perform logic functions. The CMOS-based multiplexers have leakage power that tends to increase with a reduction of their dimensions. The conventional multiplexers are volatile; they can lose their logic states when the power is off. The choice of employing transmission gates in preference to pass transistors is because of its effect on dynamic range.

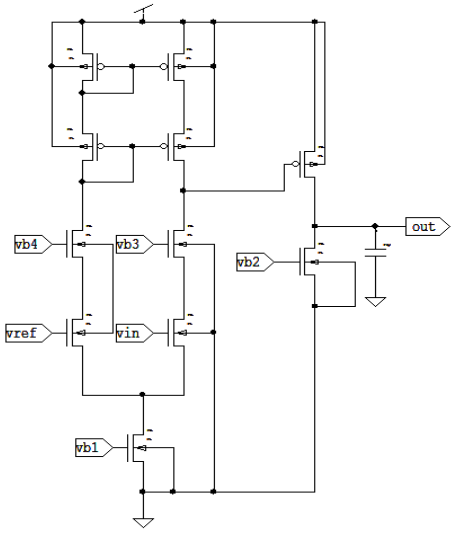

Fig.3. Schematic design of Comparator

A CMOS inverter is one of the key elements of multiplexer [7].The inverter includes a p-type MOS transistor and an n-type MOS transistor. Gate terminal of PMOS and NMOS are connected in common to serve as input terminal. Drains of PMOS and NMOS are connected in common to serve as output terminal. The multiplexer comprises of transmission gates which make the multiplexer non-restoring.

Transmission gate consists of NMOS and PMOS connected in parallel.The input terminal of the gate is composed by source terminals of the transistors PMOS and NMOS connected in common. The output terminal of the transmission gate is made of drain terminals of PMOS and NMOS also connected in common.

Selection signals S and S′ are applied to gate terminals of PMOS and NMOS transistors respectively. The select signal S and its complement S′ can enable simultaneously one of the two transmission gates at any given time when both the PMOS and NMOS transistors of the gate are on. The magnitude of input signals is substantially similar to value of V_{dd} or V_{ss} when logic 1 or logic 0respectively is applied to the input terminals.Fig.4 presents the schematic of 2 to 1 multiplexer. This multiplexer is preceded by a set of three NMOS transistors (M1, M2 and M3) for providing the input (V/4 and 3 V/4) to the 2 to1 multiplexer which is required for 2 to 1 multiplexer as can be seen from Fig. 2.

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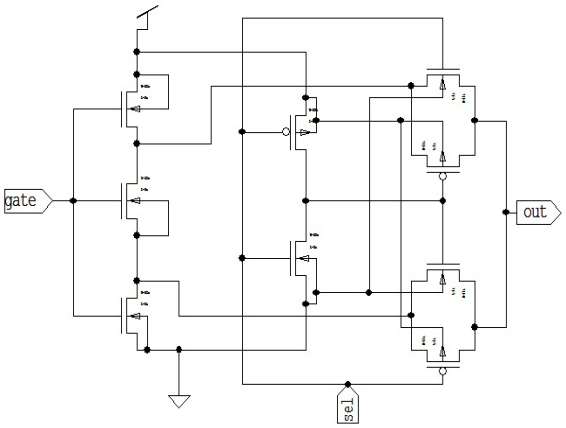

Fig.4. Schematic design of 2 to 1 Multiplexer

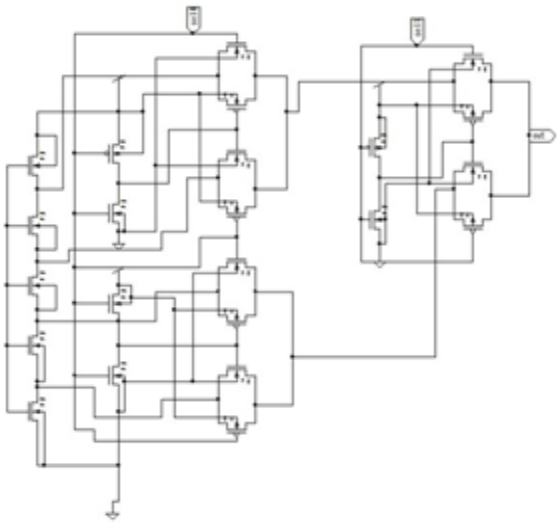

Fig.5. Schematic design of 4 to 1 Multiplexer

Fig.5. presents the schematic design of 4 to 1 analog multiplexer. Here five NMOS transistors (M1, M2, M3, M4and M5) are used for providing four different reference voltages as required by 4 to 1 multiplexer.It requires four inputs and two selection lines inputs and two selection lines.

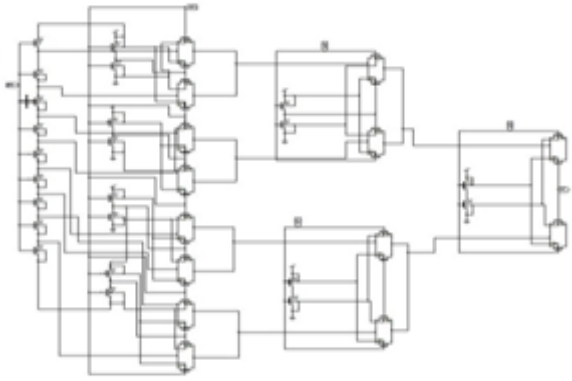

Fig.6. Schematic design of 8 to 1 Multiplexer

The schematic design of 8 to 1 multiplexer is shown in Fig.6.It requires eight inputs and three selection lines.

IV. Simulation Results

The proposed flash ADC is implemented in 0.18µm technology and simulated using Tanner T-Spice simulator. The design operates at 1.2V supply voltage.Fig.7 shows the simulated waveform of comparator. It can be seen that the output of comparator is high when the input voltage is greater than reference voltage and the output is low when the input voltage is lesser than the given reference voltage. Since comparator is the basic component of an ADC the design is made such that it consumes minimum power for operation.

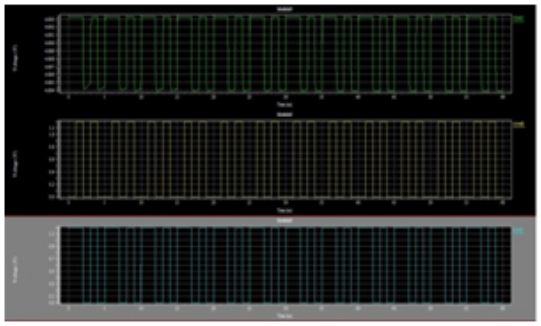

Fig.7. Simulated waveform of comparator

The dc transfer analysis is shown in Fig.8. The change in output voltage with respect to input voltage is observed at minimum voltage of 0.14V and at maximum voltage of 0.98V.

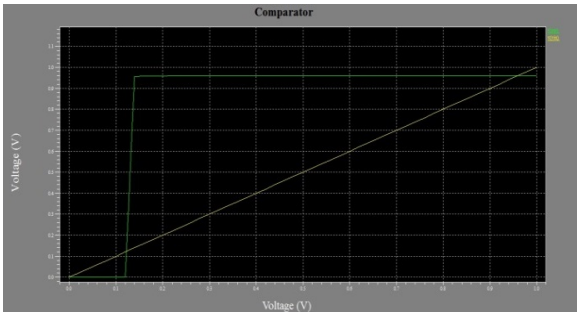

Fig.8. DC transfer analysis of comparator

Fig.9 shows the simulated waveform of 2 to 1 multiplexer, in which the output is produced according to the selection line provided.

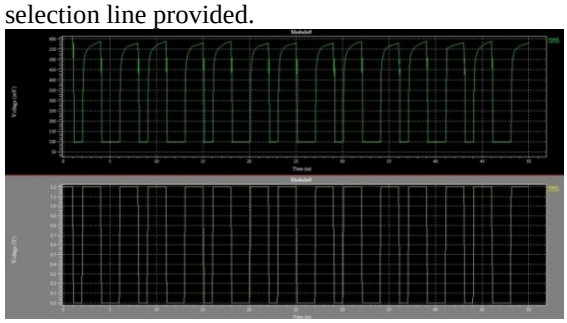

Fig.9. Simulated waveform of 2 to 1 multiplexer

The simulated waveform of 4 to 1 multiplexer is shown in Fig.10 with two selection lines at the bottom and the output is at the top of the waveform. From the result it is seen that the output raises by one LSB when any one of the two selection line is high, indicating the correct operation of the circuit.

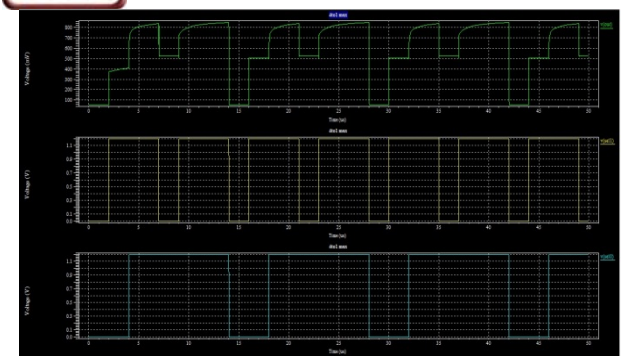

Fig.10. Simulated waveform of 4 to 1 multiplexer

Fig.11 shows the simulated waveform of 8 to 1 multiplexer with three selection line at the bottom of the waveform. The output increases or decreases by one least significant bit according to the selection line provided. When the selection line is made high the output rises by one least significant byte, when the selection line is made low, then the output decreases by one LSB thus justifying the operation.

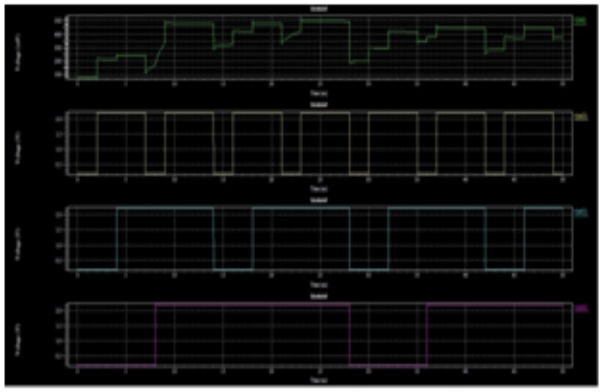

Fig.11. Simulated waveform of 8 to 1 multiplexer

The simulated output of proposed ADC architecture for sine input of 128MHz is shown in Fig.12.The sampling rate of 2Gs/s can be achieved using proposed architecture. The input voltage is compared with the reference voltage which is provided according to previous significant bit and the bit values are decided sequentially. First the bit b3 is taken by comparing input with the reference voltage. Next bit b2 is produced by checking the status of bit b3 along with the simultaneous comparison of input voltage with reference voltage. For the next bit b1 the status of bit b3 and b2 is checked along with comparison of input voltage with reference. Similarly the bit b0 is produced at the output after checking the status of bits b3, b2, b1 and comparison between input and reference voltage provided.

The delay value of comparator and multiplexers is less and hence all comparisons are done at one clock cycle conversion of flash ADC.

The power dissipation is about 2.15mW.Table I shows the comparison drawn between different types of flash ADC's.

Table I: Comparison Of Flash ADC's

ADC Type	Proposed	[8]	[9]	[10]
Resolution	4	3	4	5
Technology	0.18µm	0.18µm	130nm	0.25µm
Sampling rate	2Gsps	-	2.5Gsps	555Msps
Supply voltage(V)	1.2	1.3	1.2	2.5
Power(mW)	2.15	36.2	23.7	11.5

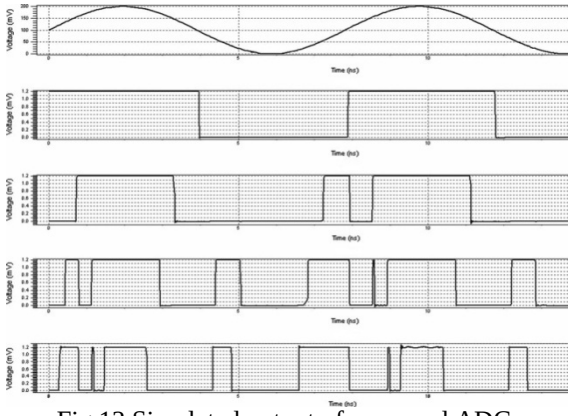

Fig.12.Simulated output of proposed ADC

V. CONCLUSION

A 4-bit ADC with reduced comparator is designed and simulated using 0.18µm CMOS technology. The proposed architecture operates at a low voltage of 1.2V and consumes only minimum power of 2.15mW. The architecture with reduced number of comparators makes it useful in portable ECG systems which operate at low voltage and at low frequency range. This architecture can be applied in System-on-Chip (SoC) applications.

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